UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/823,316 | 03/30/2001 | Morten Damgaard | 050321-1870 | 8146 |

24504 7590 03/29/2005

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

| EXAMINER | |
|---|---|
| TSE, YOUNG TOI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2637 | |

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/823,316 | DAMGAARD ET AL. | |
| | Examiner | Art Unit | |
| | YOUNG T. TSE | 2637 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-31* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *062002,072202,0519*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because the block pertaining element (210) in both Figure 2 and Figure 8 needs to have descriptive label, in conformance with 37 CFR 1.84(n) and 1.84(o). For example, a descriptive label of "R-DIVIDER" should be inserted into Figures 2 and 8 to properly describe element (210).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

2. The disclosure is objected to because of the following informalities: on page 21, line 3, "signal 208" and "FIG.7" should be "circuit 208" and "FIG.4", respectively. Appropriate correction is required.

### *Claim Objections*

3. Claims 5, 15, 20-24, and 31 are objected to because of the following informalities:

In claim 5, line 6 and line 8, "the oscillator" should be "the controllable oscillator".

In claim 15 (line 4) and claim 31 (lines 4-5), "a control signal" should be "the control signal".

In claim 20, line 9, "frequency;" should be "frequency; and".

Wherein claims 21-24 are depended upon claim 20.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, line 1, the phrase "the logic" lacks antecedent basis.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4, 7-9, 11-13, 15-18, 20-22 and 24-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Martin et al. (Applicants cited).

Martin et al. (U.S. Patent No. 5,686,864) discloses a frequency synthesizer 100 in Figure 1 for providing multiple selectable voltage controlled oscillator (VCO) frequency ranges. The frequency synthesizer 100 comprises a phase locked loop (PLL) circuit including a phase detector 104, a loop filter 110, a variable VCO 112, a buffer 116, and a loop divider 106; a VCO control circuit 114; and a lock detector 118. See column 1, line 63 to column 2, line 34.

With respect to claims 1, 7, 16, 25 and 28-30, the VCO 112 corresponds to the controllable oscillator configured to generate an output signal from one of the VCO1-VCOn based on a selected control signal from the VCO control circuit 114 and the VCO control circuit 114 corresponds to the frequency control circuit configured to generate a control signal to control the frequency of the VCO1-VCOn based on the phase difference detected from the phase detector 104. In addition to claims 25 and 28, although Martin does not explicitly show or suggest a computer readable medium for controlling the frequency of the output signal of the VCO 112, it is well known to an average person skill in the art to know that the frequency of a controllable oscillator is

capable of operating or controlling by a microprocessor or a computer readable medium.

With respect to claims 11-13 and 20-22, the frequency synthesizer 100 receives information associated with a reference frequency; the phase detector 104, the loop filter 110, the lock detector 118 and the VCO control circuit 114 determine a current frequency of the output signal of the VCO 112; the phase detector 104 compares the reference frequency to the current frequency; and the VCO control circuit 114 selects, based on the comparison of the reference frequency to the current frequency, one of selection operational states, the selected operational state having a distinct frequency which better approximates the reference frequency.

With respect to claims 4, 8-9, 17-18 and 26-27, the phase detector 104, the loop filter 110, the loop divider 106, the lock detector 118 and the VCO control circuit 114 may consider as the logic implement a binary search algorithm to determine which of the plurality of distinct frequencies for the output signal corresponding to the selection operational states best approximates the reference frequency.

With respect to claims 15, 24 and 31, the phase locked loop of the frequency synthesizer 100 repeats a number of cycles until the reference frequency is aligned or locked with a feedback frequency from the loop divider 106.

8. Claims 1, 4, 7-9, 11-13, 15-18, 20-22 and 24-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Taketoshi et al..

Taketoshi et al. (U.S. Patent No. 5,389,898) discloses a phase locked loop (PLL) circuit in Figure 7 comprising a phase detector 1, a loop filter 2, a variable voltage

control oscillator (VCO) 3 having three oscillators VCO1-VCO3, a counter 5, a shift register 6, a VCO controller 10, and a loop divider 7. See column 6, line 48 to column 7, line 28. Notice, it is well known to a person skill in the art that a PLL circuit is part of a frequency synthesizer.

With respect to claims 1, 7, 16, 25 and 28-30, the VCO 3 corresponds to the controllable oscillator configured to generate an output signal from one of the VCO1-VCO3 based on a selected control signal from the shift register 6 and the VCO controller 10; and the shift register and the VCO controller 10 correspond to the frequency control circuit configured to generate a control signal to control the frequency of the VCO1-VCO3 based on the phase difference detected from the phase detector 1. In addition to claims 25 and 28, although Taketoshi does not explicitly show or suggest a computer readable medium for controlling the frequency of the output signal of the VCO 3, it is well known to an average person skill in the art to know that the frequency of a controllable oscillator is capable of operating or controlling by a microprocessor or a computer readable medium.

With respect to claims 11-13 and 20-22, the PLL circuit receives information associated with a reference frequency; the phase detector 1, the loop filter 2, the counter 5, the shift register 6, and the VCO controller 10 determine a current frequency of the output signal of the VCO 3; the phase detector 1 compares the reference frequency to the current frequency; and the shift register 6 and the VCO controller 10 select, based on the comparison of the reference frequency to the current frequency,

one of selection operational states, the selected operational state having a distinct frequency which better approximates the reference frequency.

With respect to claims 4, 8-9, 17-18 and 26-27, the phase detector 1, the loop filter 2, the counter 5, the shift register 6, the VCO controller 10, and the loop divider 7 may consider as the logic implement a binary search algorithm to determine which of the plurality of distinct frequencies for the output signal corresponding to the selection operational states best approximates the reference frequency.

With respect to claims 15, 24 and 31, the PLL circuit repeats a number of cycles until the reference frequency is aligned or locked with a feedback frequency from the loop divider 7.

### *Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. in view of Rozenblit et al..

The claimed subject matter of claim 6 is clearly shown in Figure 1 of Martin's frequency synthesizer and discussed in paragraph 7 above. However, Martin fails to show or suggest that the frequency synthesizer is used in a communication device for use in a communication system comprising a transceiver configured to communicate with the communication system via a communication channel at a channel frequency and a frequency synthesizer configured to select the communication channel.

Rozenblit et al. (U.S. Patent No. 6,801,784 B1) discloses a communication device 100 in Figure 1 comprising at least a baseband subsystem 110 and an RF subsystem 130. The RF subsystem 130 comprises a transceiver for transmitting/ receiving data to/from the baseband subsystem 110 and a frequency synthesizer 148 for providing frequencies to a down converter circuit 178 and an up converter circuit 154 of the transceiver.

Therefore, it would have been obvious to one of ordinary skill in the art that Martin's frequency synthesizer may be able to use in a transceiver as taught by Rozenblit in order to provide frequencies to both a transmitter circuit and a receiver circuit of the transceiver.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taketoshi et al. in view of Rozenblit et al..

The claimed subject matter of claim 6 is clearly shown in Figure 7 of Taketoshi's PLL circuit or frequency synthesizer and discussed in paragraph 8 above. However, Taketoshi fails to show or suggest that the frequency synthesizer is used in a communication device for use in a communication system comprising a transceiver configured to communicate with the communication system via a communication channel at a channel frequency and a frequency synthesizer configured to select the communication channel.

Rozenblit et al. (U.S. Patent No. 6,801,784 B1) discloses a communication device 100 in Figure 1 comprising at least a baseband subsystem 110 and an RF subsystem 130. The RF subsystem 130 comprises a transceiver for transmitting/ receiving data to/from the baseband subsystem 110 and a frequency synthesizer 148 for providing frequencies to a down converter circuit 178 and an up converter circuit 154 of the transceiver.

Therefore, it would have been obvious to one of ordinary skill in the art that Taketoshi 's PLL circuit or frequency synthesizer may be able to use in a transceiver as taught by Rozenblit in order to provide frequencies to both a transmitter circuit and a receiver circuit of the transceiver.

13. Claims 3, 10, 14, 19, and 23 are ejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. in view of Rotzoll et al. (Applicants cited).

Martin fails to show or suggest the detailed embodiment of the VCO 112, which comprises a plurality of parallel capacitors capable of being engaged by the plurality of the control signals as recited in claims 3, 10, 14, 19, and 23.

Rotzoll et al. (U.S. Patent No. 5,625,325) also discloses a PLL circuit of a frequency synthesizer comprising a phase detector 71, a loop filter 750, a VCO 75 and a frequency processing circuit 72. The VCO 75 clearly includes a plurality of parallel capacitors 701-703 capable of being engaged by a digital control signal 731.

Therefore, it would have been obvious to one of ordinary skill in the art that Martin's VCO 112 is capable of including the plurality of parallel capacitors 701-703 being engaged by the digital control signal 731 as taught by Rotzoll in order to control the frequency of the VCO 75.

14. Claims 3, 10, 14, 19, and 23 are ejected under 35 U.S.C. 103(a) as being unpatentable over Taketoshi et al. in view of Rotzoll et al. (Applicants cited).

Taketoshi fails to show or suggest the detailed embodiment of the VCO circuit 3, which comprises a plurality of parallel capacitors capable of being engaged by the plurality of the control signals as recited in claims 3, 10, 14, 19, and 23.

Rotzoll et al. (U.S. Patent No. 5,625,325) also discloses a PLL circuit of a frequency synthesizer comprising a phase detector 71, a loop filter 750, a VCO 75 and a frequency processing circuit 72. The VCO 75 clearly includes a plurality of parallel capacitors 701-703 capable of being engaged by a digital control signal 731.

Therefore, it would have been obvious to one of ordinary skill in the art that Taketoshi 's VCO circuit 3 is capable of including the plurality of parallel capacitors 701-703 being engaged by the digital control signal 731 as taught by Rotzoll in order to control the frequency of the VCO 75.

***Allowable Subject Matter***

15. Claims 2 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to show or suggest that the frequency control circuit of a PLL circuit or a frequency synthesizer comprises a frequency detector, a comparator compares the output frequency of a variable oscillator to a predefined frequency, and logic determine which of a plurality of distinct frequency for the output frequency corresponding to a plurality of operational states best approximates the predefined frequency.

***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bonneau et al. discloses a state machine in responsive to a first and second counting circuit for selecting a VCO frequency range among the plurality of VCO frequency ranges such that the VCO free-running frequency obtained through the selected range gives the closest value to the reference frequency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday and Wednesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE
Primary Examiner
Art Unit 2637